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Notice of Allowability	Application No.	Applicant(s)	
	10/632,653	GEFFKEN ET AL.	
	Examiner	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the request for reconsideration filed on 14 February 2005.
2. ☒ The allowed claim(s) is/are 15-40.
3. ☒ The drawings filed on 14 February 2005 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

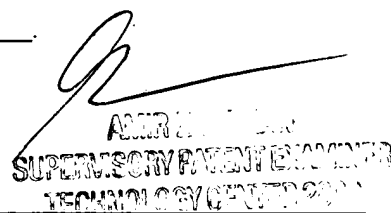
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|---|--|
| <ol style="list-style-type: none"> 1. <input type="checkbox"/> Notice of References Cited (PTO-892) 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. <input type="checkbox"/> Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date _____ 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit
of Biological Material | <ol style="list-style-type: none"> 5. <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) 6. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date _____ 7. <input type="checkbox"/> Examiner's Amendment/Comment 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance 9. <input type="checkbox"/> Other _____ |
|---|--|


 SUPERVISORY PATENT EXAMINER
 TECHNOLOGY CENTER

DETAILED ACTION

This office action is in response to the filing of the request for reconsideration on 14 February 2005. Claims 15-40 are pending.

Drawings

The drawings were received on 14 February 2005. These drawings are approved by the examiner.

Allowable Subject Matter

Claims 15-40 are allowed.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance: prior art does not anticipate, teach, or suggest a method for forming an electronic structure where a substrate layer includes a first electronic device; forming a passivating layer on the substrate layer and in mechanical contact with the substrate layer, wherein the passivating layer is on the first electronic device and is in mechanical contact with the first electronic device; forming a first insulative layer on the passivating layer and in mechanical contact with the passivating layer; forming a first damascene conductive wire/stud in the first insulative layer; removing a top portion of the first insulative layer such that an upper portion of the first damascene conductive wire/stud is above the first insulative layer after the removing; forming a metallic capping layer on the first insulative

layer such that the metallic capping layer is in conductive contact with the first damascene conductive wire/stud; subtractively etching a portion of the metallic capping layer to form a subtractive etch metallic cap on the upper portion of the first damascene conductive wire/stud such that the subtractive etch metallic cap is in conductive contact with the first damascene conductive wire/stud; forming a second insulative layer on the first insulative layer, wherein the second insulative layer covers the subtractive etch metallic cap; and forming a damascene conductive wiring line structure within the second insulative layer such that the damascene conductive wiring line structure is above the subtractive etch metallic cap and conductively coupled to the subtractive etch metallic cap.

For example, Applicant's prior art discloses a method for forming an electronic structure where a substrate layer that includes a first electronic device; forming a passivating layer on the substrate layer and in mechanical contact with the substrate layer, wherein the passivating layer is on the first electronic device and is in mechanical contact with the first electronic device; forming a first insulative layer on the passivating layer and in mechanical contact with the passivating layer; forming a first damascene conductive wire/stud in the first insulative layer; forming a second damascene conductive wire/stud in the first insulative layer such that a lower portion of the second damascene conductive wire/stud is conductively coupled to a second portion of the first electronic device; forming a second insulative layer on the first insulative layer; and forming a damascene conductive wiring line structure within the second insulative layer.

However, Applicant's prior art does not disclose, anticipate, teach, or suggest removing a top portion of the first insulative layer such that an upper portion of the first damascene conductive wire/stud is above the first insulative layer after the removing; forming a metallic capping layer on the first insulative layer such that the metallic capping layer is in conductive contact with the first damascene conductive wire/stud; subtractively etching a portion of the metallic capping layer to form a subtractive etch metallic cap on the upper portion of the first damascene conductive wire/stud such that the subtractive etch metallic cap is in conductive contact with the first damascene conductive wire/stud.

Joshi et al. (6,323,554) disclose a method for forming an electronic structure where a substrate layer that includes a first electronic device; forming a first insulative layer on the first electronic device and substrate layer; forming a first damascene conductive wire/stud in the first insulative layer; forming a second insulative layer on the first insulative layer; and forming a damascene conductive wiring line structure within the second insulative layer.

However, Joshi et al. do not disclose, anticipate, teach or suggest forming a passivating layer on the substrate layer and in mechanical contact with the substrate layer, wherein the passivating layer is on the first electronic device and is in mechanical contact with the first electronic device; removing a top portion of the first insulative layer such that an upper portion of the first damascene conductive wire/stud is above the first insulative layer after the removing; forming a metallic capping layer on the first insulative layer such that the metallic capping layer is in conductive contact with the first

damascene conductive wire/stud; subtractively etching a portion of the metallic capping layer to form a subtractive etch metallic cap on the upper portion of the first damascene conductive wire/stud such that the subtractive etch metallic cap is in conductive contact with the first damascene conductive wire/stud.

Zhou et al. (6,376,353) disclose a method for forming an electronic structure where a substrate layer that includes a first electronic device; forming a passivating layer on the substrate layer and in mechanical contact with the substrate layer; forming a first insulative layer on the passivating layer and in mechanical contact with the passivating layer; forming a first damascene conductive wire/stud in the first insulative layer; forming a metallic capping layer on the first insulative layer such that the metallic capping layer is in conductive contact with the first damascene conductive wire/stud; subtractively etching a portion of the metallic capping layer to form a subtractive etch metallic cap on the upper portion of the first damascene conductive wire/stud such that the subtractive etch metallic cap is in conductive contact with the first damascene conductive wire/stud.

However, Zhou et al. do not disclose, anticipate, teach or suggest removing a top portion of the first insulative layer such that an upper portion of the first damascene conductive wire/stud is above the first insulative layer after the removing; forming a second insulative layer on the first insulative layer, wherein the second insulative layer covers the subtractive etch metallic cap; and forming a damascene conductive wiring line structure within the second insulative layer such that the damascene conductive

wiring line structure is above the subtractive etch metallic cap and conductively coupled to the subtractive etch metallic cap.

The prior art made of record in this action does not anticipate, teach, or suggest a method for forming an electronic structure where a substrate layer includes a first electronic device; forming a passivating layer on the substrate layer and in mechanical contact with the substrate layer, wherein the passivating layer is on the first electronic device and is in mechanical contact with the first electronic device; forming a first insulative layer on the passivating layer and in mechanical contact with the passivating layer; forming a first damascene conductive wire/stud in the first insulative layer; removing a top portion of the first insulative layer such that an upper portion of the first damascene conductive wire/stud is above the first insulative layer after the removing; forming a metallic capping layer on the first insulative layer such that the metallic capping layer is in conductive contact with the first damascene conductive wire/stud; subtractively etching a portion of the metallic capping layer to form a subtractive etch metallic cap on the upper portion of the first damascene conductive wire/stud such that the subtractive etch metallic cap is in conductive contact with the first damascene conductive wire/stud; forming a second insulative layer on the first insulative layer, wherein the second insulative layer covers the subtractive etch metallic cap; and forming a damascene conductive wiring line structure within the second insulative layer such that the damascene conductive wiring line structure is above the subtractive etch metallic cap and conductively coupled to the subtractive etch metallic cap.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

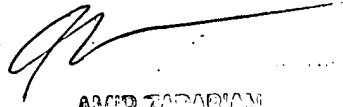
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP


AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
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